Claim Amendments

Please amend claims 1, 3-7, 9, 10, 12, 14-17, 19, and 20 as follows.

Please cancel claims 8, 13, and 18 as follows.

Please add new claims 21-23 as follows.

1. (currently amended) A ~~plasma etching~~ dual damascene formation method for ~~improving an~~ reducing a faceted etching profile at a trench/via interface comprising the steps of:

providing a substrate ~~including~~ comprising a[n] ~~oxide containing~~ dielectric insulating layer ~~in a multilayer semiconductor device~~;

providing a first patterned photoresist layer exposing an uppermost layer of the substrate for ~~anisotropically~~ plasma etching a first opening;

~~anisotropically~~ plasma etching through a first thickness ~~of at least a~~ portion of the ~~substrate~~ dielectric insulating layer to form the first opening;

removing the first patterned photoresist layer;

blanket depositing an etching stop liner to ~~cover at least a portion of~~ line the sidewalls of the first opening;

at least partially filling the first opening with a plug of resinous material;

photolithographically patterning ~~according to a photolithographic process~~ a second photoresist layer for etching a second opening at least partially overlying and encompassing the first opening; and,

~~anisotropically~~ plasma etching through ~~at least another~~ a second thickness portion of the ~~thickness of the substrate~~ dielectric insulating layer ~~including the first opening~~ to form [a] the second opening ~~at least partially overlying a remaining portion of the first opening~~.

2. (original) The method of claim 1, wherein the first opening comprises a via opening and the second opening comprises a trench line opening to form a dual damascene structure.

3. (currently amended) The method of claim 2, wherein the dual damascene structure comprises a trench portion and via portion having a via/trench interface ~~formed in a continuous portion of the oxide containing~~ comprising the dielectric insulating layer.

4. (currently amended) The method of claim 1, wherein the step of blanket depositing ~~includes~~ comprises depositing the etching stop liner to conformally cover ~~at least~~ the sidewall and bottom portions of the first opening.

5. (currently amended) The method of claim 1, wherein the etching stop liner ~~includes at least one~~ is selected from the group consisting of a ~~metal~~ nitride and a ~~metal~~ carbide.

6. (currently amended) The method of claim 1 [5], wherein the etching stop liner ~~includes~~ is selected from the group consisting ~~at least one~~ of silicon nitride, silicon carbide, silicon oxynitride, and titanium nitride.

7. (currently amended) The method of claim 6 [5], wherein the etching stop liner is formed ~~over~~ having a thickness of about 50 Angstroms to about 500 Angstroms.

8. (cancelled)

9. (currently amended) The method of claim [8]1, wherein the plug is at least partially filled to a level in the first opening ~~to a level at least~~ about equal to a ~~predetermined~~ depth of the subsequently formed second opening ~~formed during the step of anisotropically plasma etching through the at least another portion~~.

10. (currently amended) The method of claim 1 [8], wherein the plug is ~~formed of at least one~~ selected from the group consisting of a resinous polymer and a photosensitive resinous polymer.

11. (original) The method of claim 10, wherein the photosensitive resinous polymer is at least partially cured by exposure to polymerizing radiation.

12. (currently amended) A ~~plasma etching~~ dual damascene formation method in a single dielectric insulating layer for ~~improving an etching profile~~ reducing facet formation at a via/trench interface ~~in a dual damascene structure~~ comprising the steps of:

providing a substrate ~~including~~ comprising a[n] ~~oxide containing~~ dielectric insulating layer ~~in a multilayer semiconductor device~~;

providing a first patterned photoresist layer exposing an uppermost layer of the substrate for ~~anisotropically~~ plasma etching a via opening;

~~anisotropically~~ plasma etching through a first thickness ~~of at least a~~ portion of the ~~substrate~~ dielectric insulating layer to form the via opening in closed communication with an underlying conductive area;

removing the first patterned photoresist layer;

blanket depositing an etching stop liner to cover ~~at least a portion of~~ the sidewalls and bottom portion of the via opening;

at least partially filling the via opening with a via plug;

photolithographically patterning ~~according to a photolithographic process~~ a second photoresist layer for etching a trench line opening at least partially overlying and encompassing the via opening; and,

~~anisotropically~~ plasma etching through ~~at least another~~ a second thickness portion of the ~~thickness of the substrate~~ dielectric insulating layer ~~including the first opening~~ to form [a] the trench line opening ~~at least partially overlying a remaining portion of the via opening~~ to form a dual damascene structure.

13. (cancelled)

14. (currently amended) The method of claim 12, wherein the step of blanket depositing ~~includes~~ comprises depositing the etching stop liner ~~to~~ conformally ~~cover at least the sidewalls and bottom portions of the via opening~~.

15. (currently amended) The method of claim 12, wherein the etching stop liner ~~includes at least one~~ is selected from the group consisting of a ~~metal~~ nitride and a ~~metal~~ carbide.

16. (currently amended) The method of claim 12[5], wherein the etching stop liner ~~includes~~ is selected from the group consisting ~~at least one~~ of silicon nitride, silicon carbide, silicon oxynitride, and titanium nitride.

17. (currently amended) The method of claim 16[5], wherein the etching stop liner is formed ~~over~~ having a thickness of about 50 Angstroms to about 500 Angstroms.

18. (cancelled)

19. (currently amended) The method of claim 12[8], wherein the via plug is ~~at least partially~~ filled to a level in the ~~first~~ via opening ~~to a level at least~~ about equal to a ~~predetermined~~ depth of the subsequently formed trench line opening ~~formed during the step of anisotropically plasma etching through the at least another portion~~.

20. (currently amended) The method of claim 19 [8], wherein the via plug is ~~formed of at least one~~ selected from the group consisting of a resinous polymer and a photosensitive resinous polymer.

21. (new) The method of claim 1, wherein the dielectric insulating layer is selected from the group consisting of silicon oxide, doped silicon dioxide, porous oxides, xerogels, SOG (spin-on glass, polysilsesquioxane, parylene, polyimide, benzocyclobutene, amorphous Teflon, and spin-on polymer (SOP).

22. (new) The method of claim 12, wherein the dielectric insulating layer is selected from the group consisting of silicon oxide, doped silicon dioxide, porous oxides, xerogels, SOG (spin-on glass, polysilsesquioxane, parylene, polyimide, benzocyclobutene, amorphous Teflon, and spin-on polymer (SOP).

23. (new) The method of claim 12, wherein the via plug comprises a material selected from the group consisting of methyl methacrylates, polyolefins, polyacetals, polycarbonates, polypropylenes, polyimides, and oxides.